Silicon Substrate Coupling Noise Modeling, Analysis, and Experimental Verification for Mixed Signal Integrated Circuit Design

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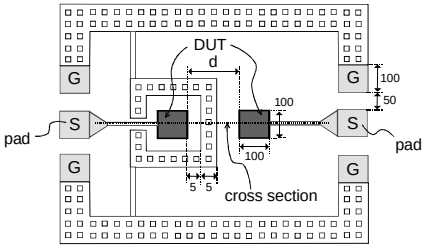
***Abstract* — The frequency-variant characteristics of silicon substrate were physically modeled, analytically investigated, and experimentally verified. The scalable circuit model parameter extraction methodology was newly developed. Thus, the proposed technique can provides the efficient performance evaluations as well as the accurate design guidelines concerned with the complicated mixed signal integrated circuit designs.**

I. INTRODUCTION

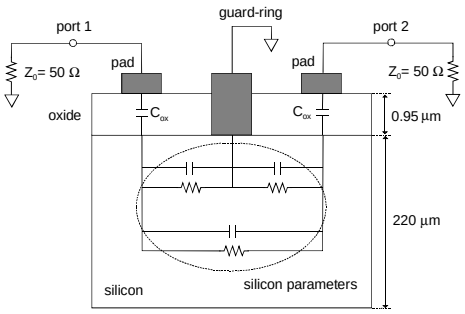
In the SOC (System On a Chip) or mixed signal ICs, the coupling noise between circuit blocks due to a conductive silicon substrate has a significant effect on sensitive RF/analog circuit performance. Thus, isolation between the sensitive or noisy circuit blocks is a crucial design issue. Using simple separation between circuits in order to reduce coupling noise costs too much. It is essential to carefully understand the physical characteristics of coupling, thereby minimizing the die area. To this date, there have been many research efforts to characterize the silicon substrate coupling-noise through the experimental techniques [1][2], numerical analyses [2]-[3], and circuit models [4]. However, these existing techniques have deficiencies in their computation time, physical interpretation, or model accuracy. In this work, a new accurate, as well as, compact physical circuit model describing silicon substrate coupling effects is presented, analyzed, and experimentally verified.

II. SUBSTRATE MODELING AND PARAMETER EXTRACTION

A physical circuit model for representing the effects of the silicon substrate was developed by using an RC network as shown in Fig. 1. Since the silicon substrate has frequency-variant characteristics, the circuit model parameters have significant effects on model accuracy. That is, for a frequency less than the first pole frequency (f_{p1}^{x}), a conductive effect is significant since the silicon substrate acts as a poor conductor at low frequency. Note, superscript x means structure type, i.e., no guard-ring (x=i), one guard-ring (x=j), and two guard-rings (x=k), respectively. In contrast, above the third zero frequency (f_{z3}^{x}), a capacitive effect is the dominant coupling



(a) A test pattern layout (one guard-ring).



(b) An equivalent circuit.

Fig. 1. A structure to investigate silicon substrate coupling.

mechanism since the substrate acts as a dielectric material at high frequency [5]. Moreover, in the moderate frequency range between the first pole and third zero, there is a transition region. The s-parameter-based circuit analyses of the equivalent circuits were performed and the results are summarized in Fig. 2. Then, the circuit model parameters were extracted by equating the measured s-

structure		w/o G/R		one G/R		two G/R		remarks
parameter		R	C	R	C	R	C	
oxide		NR	C_{ox}	NR	C_{ox}	NR	C_{ox}	
silicon	pad-to-pad	R_1^i	C_1^i	R_1^j	C_1^j	R_1^k	C_1^k	$R_1^x(d), C_1^x(d)$: scalable
	pad-to-gnd	R_2^i	C_2^i	NR	NR	NR	NR	
	pad-to-G/R	NR	NR	R_{3l}^j	C_{3l}^j	R_3^k	C_3^k	l : left side r : right side
				R_{3r}^j	C_{3r}^j			
frequency	operating	f_o^i		f_o^j		f_o^k		
	poles	f_{p1}^i, f_{p2}^i		f_{p1}^j, f_{p2}^j		f_{p1}^k, f_{p2}^k		
	zeros	$f_{z1}^i, f_{z2}^i, f_{z3}^i$		$f_{z1}^j, f_{z2}^j, f_{z3}^j$		$f_{z1}^k, f_{z2}^k, f_{z3}^k$		$f_{z1}^x = f_{z2}^x = 0$

(a) Notation of the model parameters
('NR' means 'not required', i: without guard-ring, j: with one guard-ring, k: with two guard-rings).

s-par. \ x	$x = i$ (without guard-ring)	$x = j$ (with one guard-ring)	$x = k$ (with two guard-rings)
$(S_{21})^x$	$\dfrac{-2Z_0 \cdot C_c^i \cdot s^2 \left(s+\dfrac{1}{R_1^i C_1^i}\right)}{\left(s+\dfrac{1}{R_2^i C_{ox}}\right)\left\{s+\dfrac{1}{C_{ox}}\left(\dfrac{2}{R_1^i}+\dfrac{1}{R_2^i}\right)\right\}}$	$\dfrac{-2 \cdot Z_0 \cdot s^2 \cdot C_1^j \cdot \dfrac{C_{ox}}{\left(C_{3l}^j + C_{ox}\right)} \cdot \left(s+\dfrac{1}{R_1^j \cdot C_1^j}\right)}{\left\{s+\dfrac{1}{C_{ox}}\left(\dfrac{1}{R_1^j}+\dfrac{1}{R_{3r}^j}\right)\right\}\left\{s+\dfrac{1}{\left(C_{ox}+C_{3l}^j\right)}\left(\dfrac{1}{R_1^j}+\dfrac{1}{R_{3l}^j}\right)\right\}}$	$\dfrac{-2Z_0 \cdot C_1^k \cdot s^2 \left(\dfrac{C_{ox}}{C_{ox}+C_3^k}\right)^2 \left(s+\dfrac{1}{R_1^k C_1^k}\right)}{\left\{s+\dfrac{1}{\left(C_{ox}+C_3^k\right)R_3^k}\right\}\left\{s+\dfrac{1}{\left(C_{ox}+C_3^k\right)}\left(\dfrac{1}{R_3^k}+\dfrac{2}{R_1^k}\right)\right\}}$
$\lvert S_{21}\rvert^x_{f_o^x < f_{p1}^x}$	$\dfrac{2 \cdot Z_0 \cdot \left(R_2^i\right)^2 \cdot C_{ox}^2}{2 \cdot R_2^i + R_1^i} s^2$	$\dfrac{2 \cdot Z_0 \cdot C_{ox}^2 \cdot R_1^j \cdot R_{3r}^j \cdot R_{3l}^j}{\left(R_{3r}^j + R_1^j\right)\left(R_{3l}^j + R_1^j\right)} s^2$	$\dfrac{2 \cdot Z_0 \cdot C_{ox}^2 \cdot \left(R_3^k\right)^2}{R_1^k + 2R_3^k} s^2$
$\lvert S_{21}\rvert^x_{f_{p2}^x < f_o^x < f_{z3}^x}$	$\dfrac{2 \cdot Z_0}{R_1^i}$	$\dfrac{2 \cdot Z_0}{R_1^j} \cdot \dfrac{C_{ox}}{\left(C_{3l}^j + C_{ox}\right)}$	$\dfrac{2 \cdot Z_0}{R_1^k} \cdot \left(\dfrac{C_{ox}}{C_{ox}+C_3^k}\right)^2$
$\lvert S_{21}\rvert^x_{f_{z3}^x < f_o^x}$	$2 \cdot Z_0 \cdot C_1^i \cdot s$	$2 \cdot Z_0 \cdot C_1^j \cdot \left(\dfrac{C_{ox}}{C_{ox}+C_{3l}^j}\right) \cdot s$	$2 \cdot Z_0 \cdot C_1^k \cdot \left(\dfrac{C_{ox}}{C_{ox}+C_3^k}\right)^2 \cdot s$

(b) Analytic expressions for different structures.
Fig. 2. Analytic expressions for substrate effect investigation.

TABLE I
EXTRACTED PARAMETERS FOR THE TEST PATTERNS (NR: NOT REQUIRED)

$\rho\,[\Omega \cdot cm]$	x	d[μm]	$R_1^x\,[\Omega]$	$C_1^x\,[F]$	$R_2^i\,[\Omega]$	$C_2^i\,[F]$	$R_3^k\,[\Omega]$	$C_3^k\,[F]$
5~8	i	35	8.923E+2	1.017E-14	4.700E+2	7.884E-15	NR	NR
	i	110	1.687E+3	5.481E-15	4.700E+2	7.884E-15	NR	NR
	k	110	3.950E+3	2.368E-15	NR	NR	1.984E+2	5.209E-14
25~50	i	110	8.630E+3	5.012E-15	1.838E+3	7.219E-15	NR	NR
	k	110	4.724E+4	1.251E-15	NR	NR	1.033E+3	4.747E-14
2000	i	35	2.043E+4	2.537E-15	1.033E+3	4.747E-14	NR	NR
	i	110	4.724E+4	1.251E-15	1.033E+3	4.747E-14	NR	NR

parameter-data data and circuit model analytical expressions pertinent to the characteristic frequency range. The model parameters and their extraction procedures are summarized in Fig. 3. The extracted parameters are scalable with the substrate resistivity variations and physical structure variations, i.e., spacing, size, and guard-ring effects, in a broad frequency band. Thus, the circuit performance with these parameter variations is very accurately estimated.

III. RESULT AND VERIFICATION

In order to experimentally verify the model and analyses, various test patterns were designed and fabricated by using a standard CMOS process and varying the three important parameters concerned with circuit design, i.e., silicon substrate resistivity (i.e., 5~8 $\Omega \cdot cm$, 25~50 $\Omega \cdot cm$, and 2k $\Omega \cdot cm$), isolation distance (35 μm, 60 μm, and 110 μm), and guard-ring effects (i.e., without guard-ring,

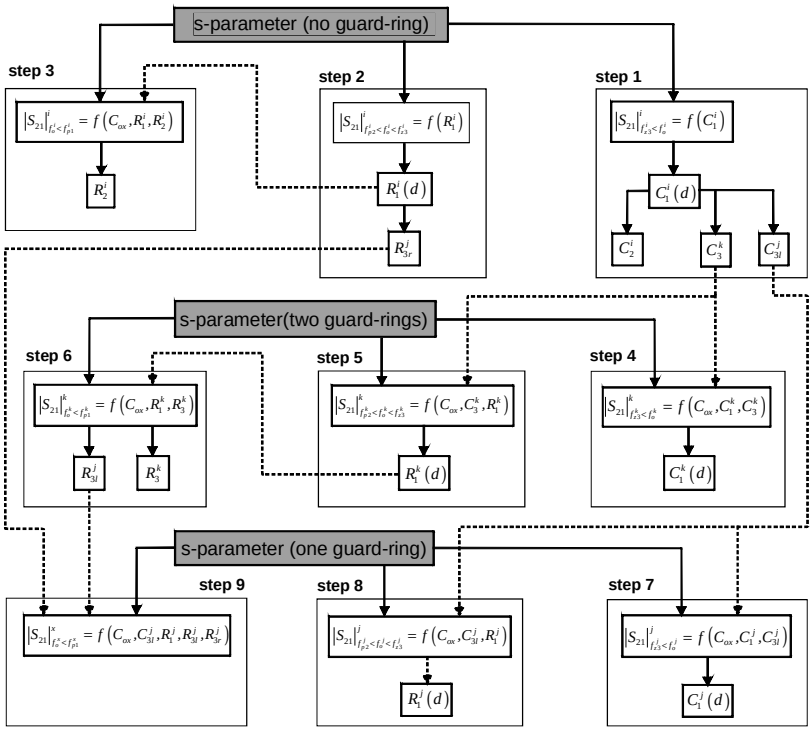
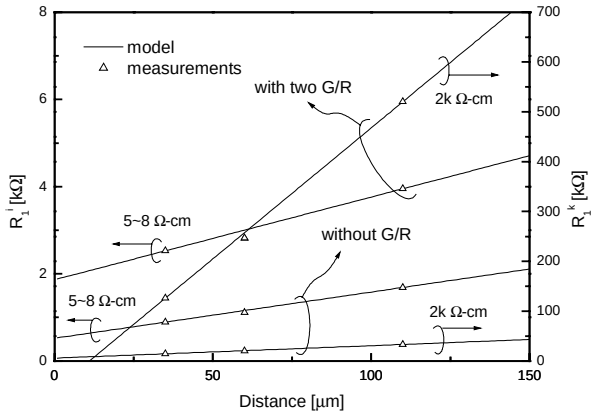


Fig. 3. Schematic description for the extraction of substrate parameters from measured s-parameters.

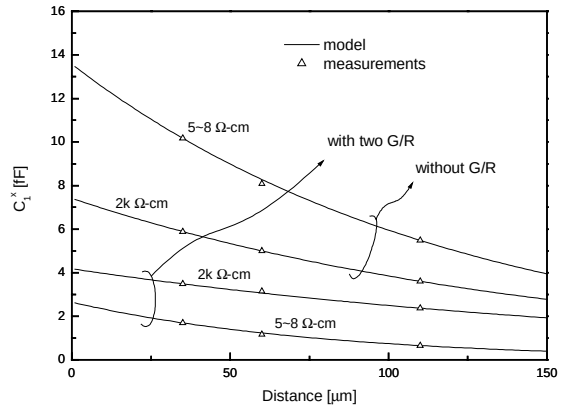
with one guard-ring, and with two guard-rings). The oxide thickness and silicon-substrate thickness are 0.95 μm and 220 μm , respectively. The layout dimensions of an example test pattern and an equivalent circuit are shown in Fig. 1. They were measured in the frequency range of 100MHz to 20GHz with a vector network analyzer. The parasitic effects during the measurements were de-embedded by using the y-parameter-based de-embedding techniques. Note, that the silicon substrate coupling is an intricate function of the operating frequency, substrate resistivity, separation distance, and guard-ring effects. The model parameters for the test structures are extracted according to the procedures shown in Fig. 3 and summarized in Table 1. The parameters are scalable with the substrate resistivity, distance, and guard-ring effects as shown in Fig. 4. With these model parameters, HSPICE-based s-parameters models and experiment-based s-parameters are compared in Fig. 5. In the interesting frequency range (about 200MHz to 15GHz), the model-based simulation results have excellent agreement with the experimental data as shown in Fig. 5.

IV. CONCLUSION

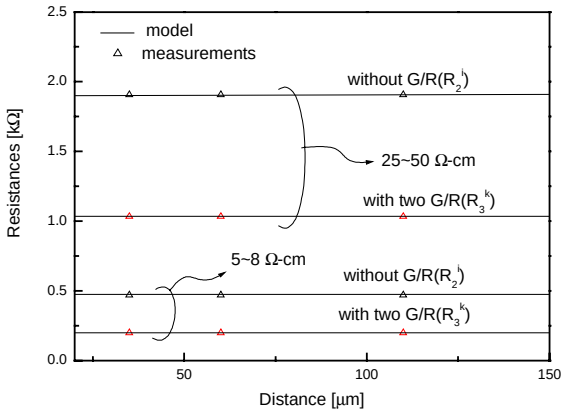
The proposed circuit model and parameter extraction methodology are extremely valuable since such intricate silicon substrate coupling phenomena can be conveniently as well as accurately estimated at the early phase of circuit design. That is, not only does the circuit model permit the efficient integral simulation including both the circuits and the silicon substrate effects with a conventional circuit simulator such as HSPICE, but also the analytical model equations provide very accurate design guidelines for circuit designers. Thus, the proposed techniques readily employed for the mixed signal IC designs.



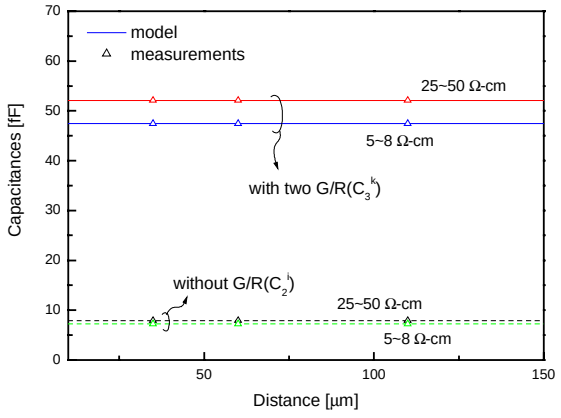
(a) Coupling resistances versus different separation distances.



(b) Coupling capacitances versus different separation distances.

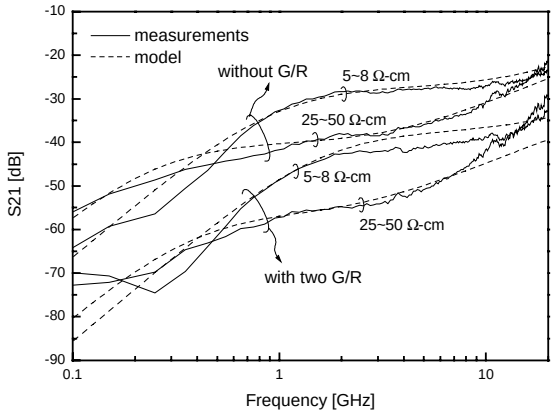


(c) DUT to ground resistances versus different distances.

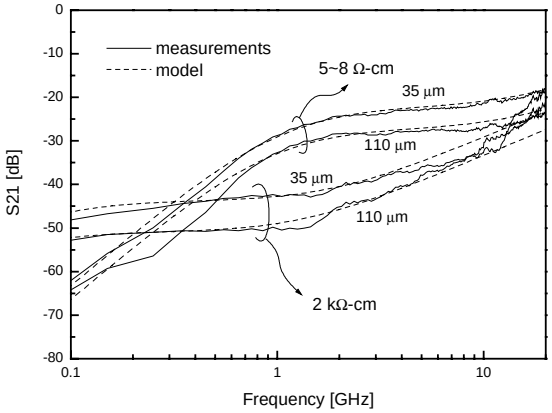


(d) DUT to ground capacitances versus different separation distances.

Fig. 4. Parameter variations with Resistivity, spacing, and guard-ring effects.



(a) Substrate coupling noise versus the substrate Resistivity. Spacing between DUT is 35um.



(b) Substrate coupling noise versus different spacing between DUTs.

Fig. 5. Comparison of the simulated s-parameters with the experimental s-parameters.

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